Future of CPU Bus Architectures

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March 26, 1998

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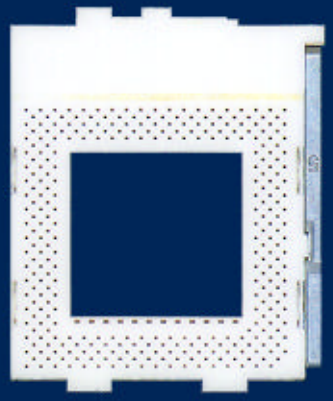
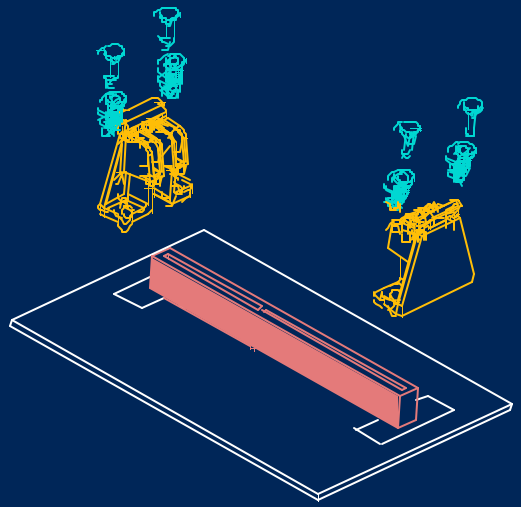
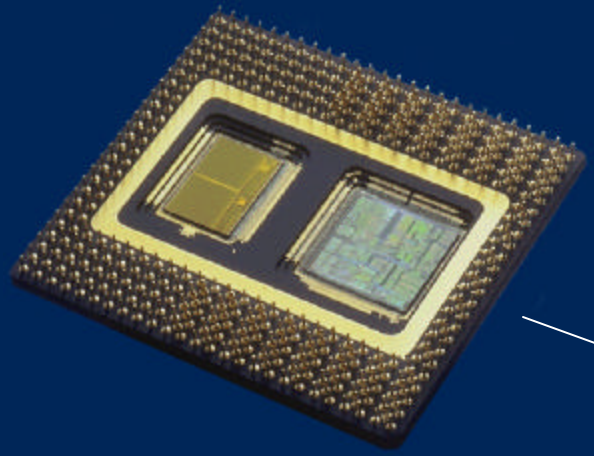
Presentation downloadable from http://developer.intel.com/solutions/CPUbus.html

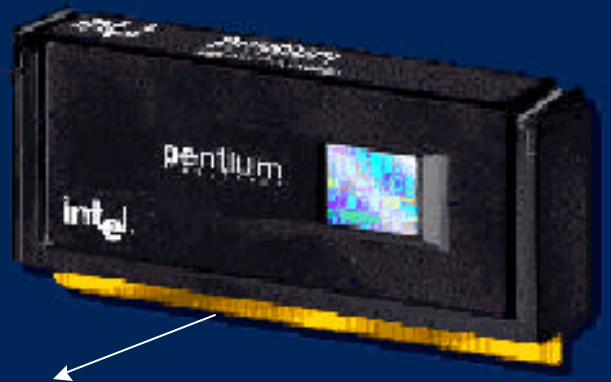
Sockets/Slots NOT the Issue



Pentium® (P5)
Processor Bus







Pentium Pro/
Pentium II
(P6) Processor Bus

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What drives bus architecture?

Agenda

- Industry Megatrends
- Addressing These Trends
- Building On A Solid Foundation

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Agenda

- Industry Megatrends
- Add
- Buil

More data being processed
More data being displayed
More data being stored
More data being streamed

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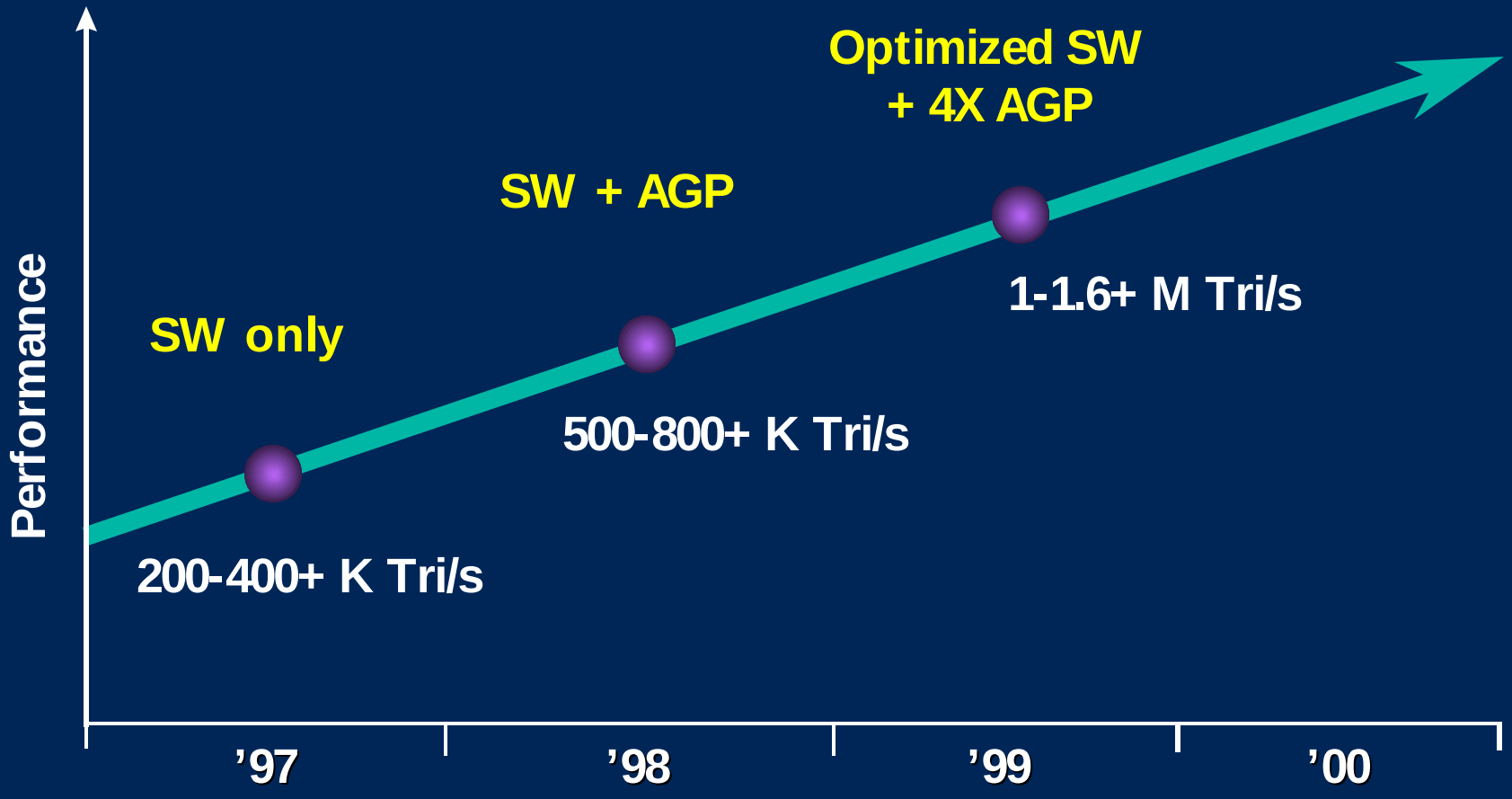
More Data Being Processed

Rich data types eg 3D



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More Data Being Processed

Rich data types eg 3D

Perf

200-400+ K Tri/s

500-800+ K Tri/s

1-1.6+ M Tri/s

10X Improvement Over 3 Years

'97 '98 '99 '00

Data Sets Are >> L2 Cache

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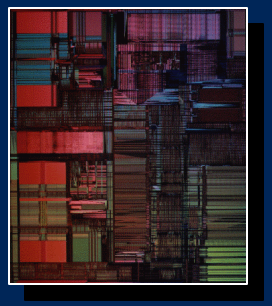
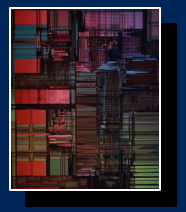
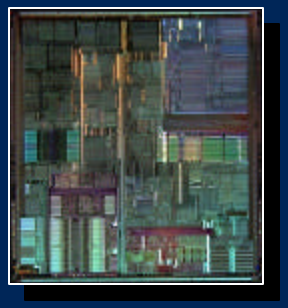
More Data Being Processed

Improving processor capability. . .

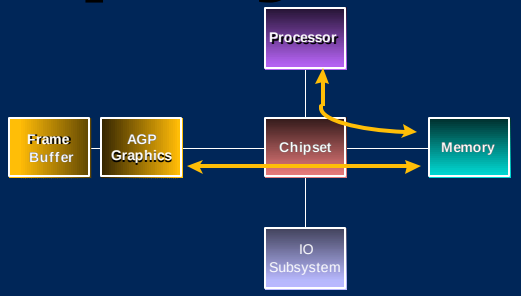
Silicon Process Technology	0.8µ 5v	0.6µ 3.3v	0.35µ 2.5v	0.25µ 1.7v	0.18µ -
P5 Technology					
P6 Technology					

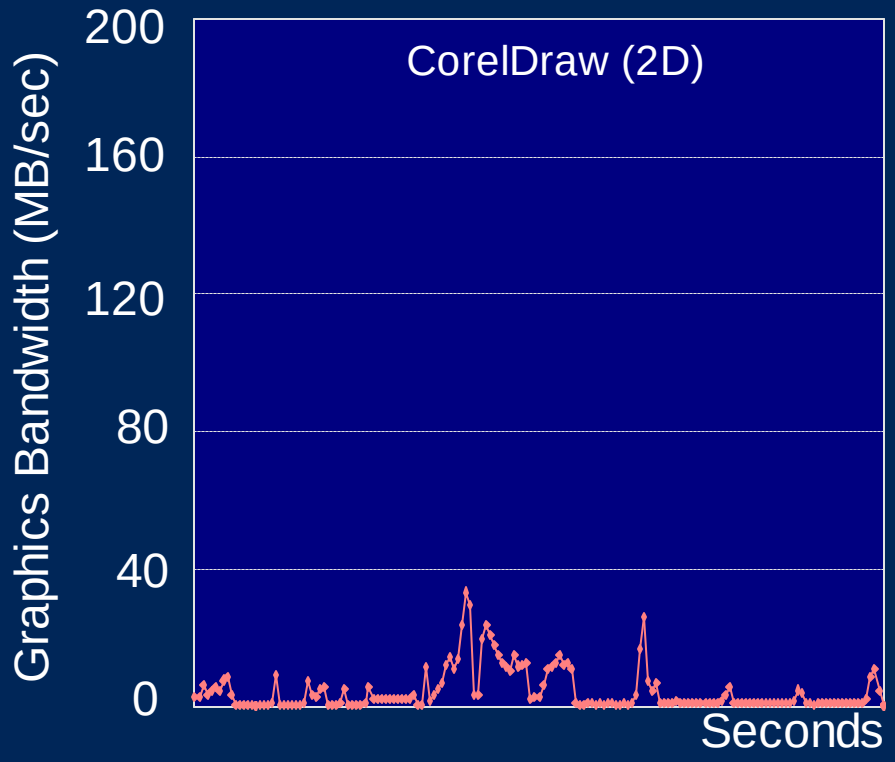
Estimated

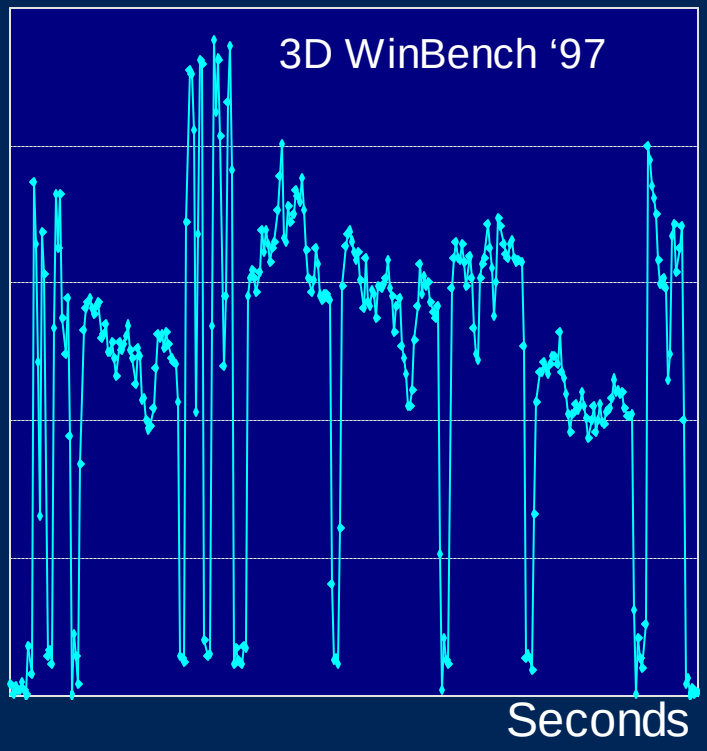
. . . but relative bus latency is increasing

More Data Being Displayed

Graphics workload





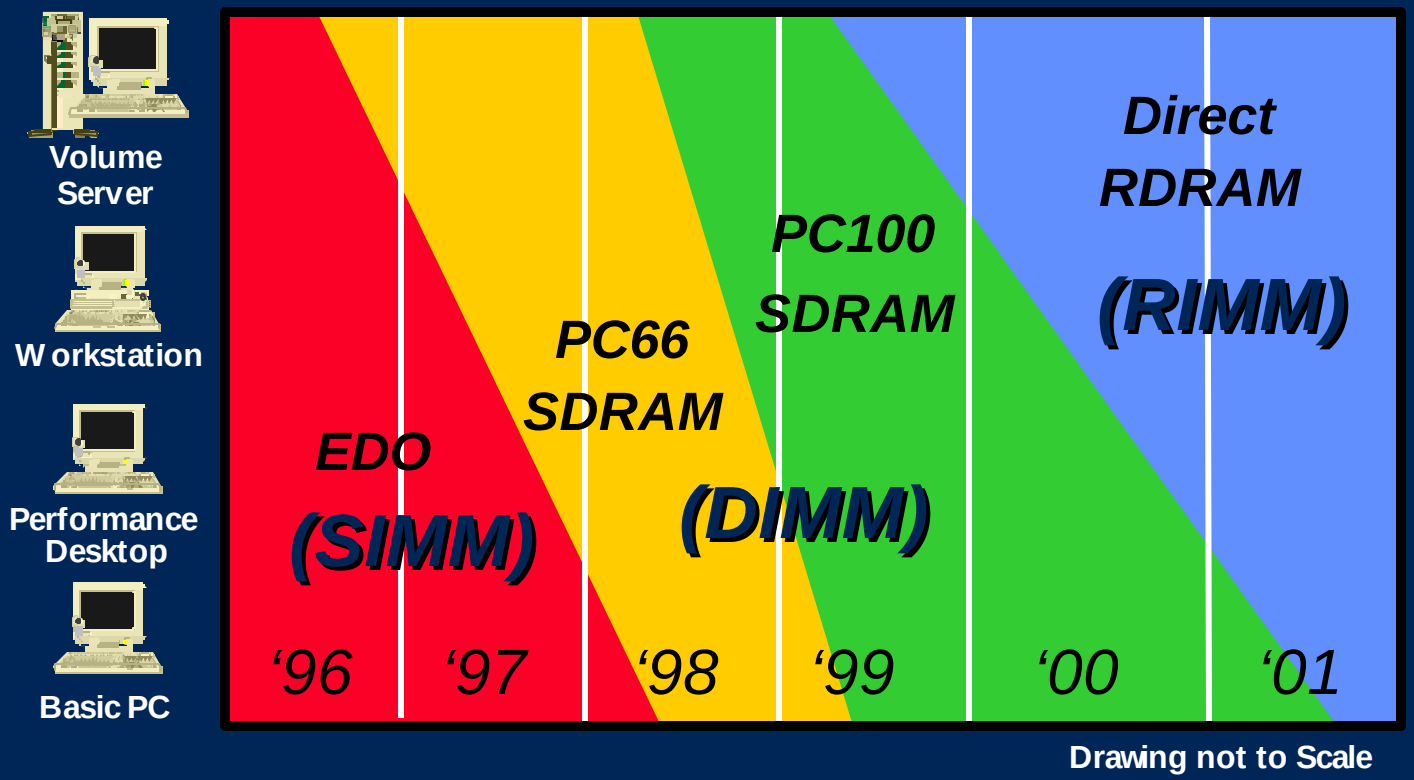


Pentium® II Processor in a 300MHz System with 66 MHz SDRAM

Contention for memory adds latency

More Data Being Stored

DRAM industry's focus is density



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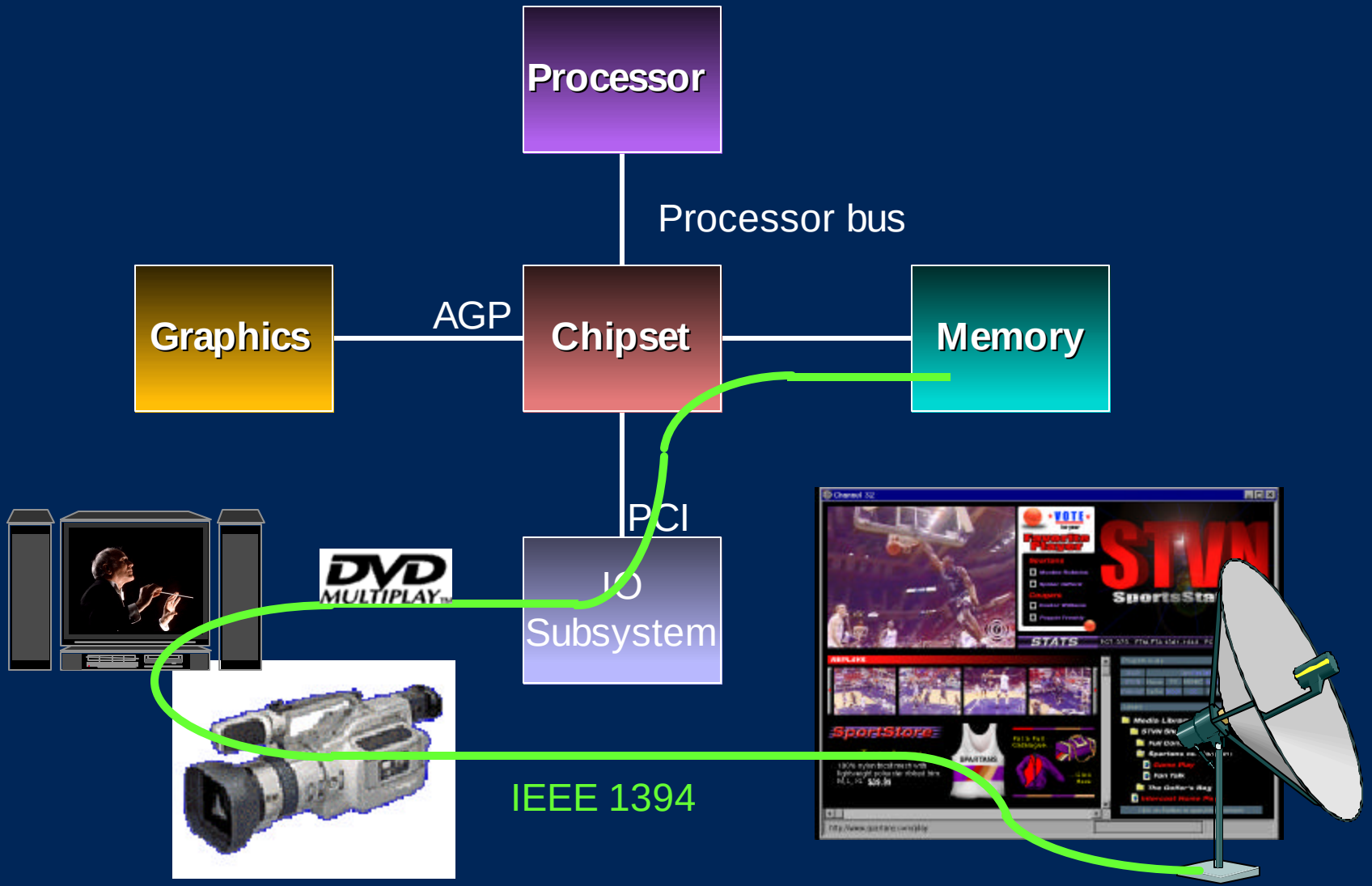
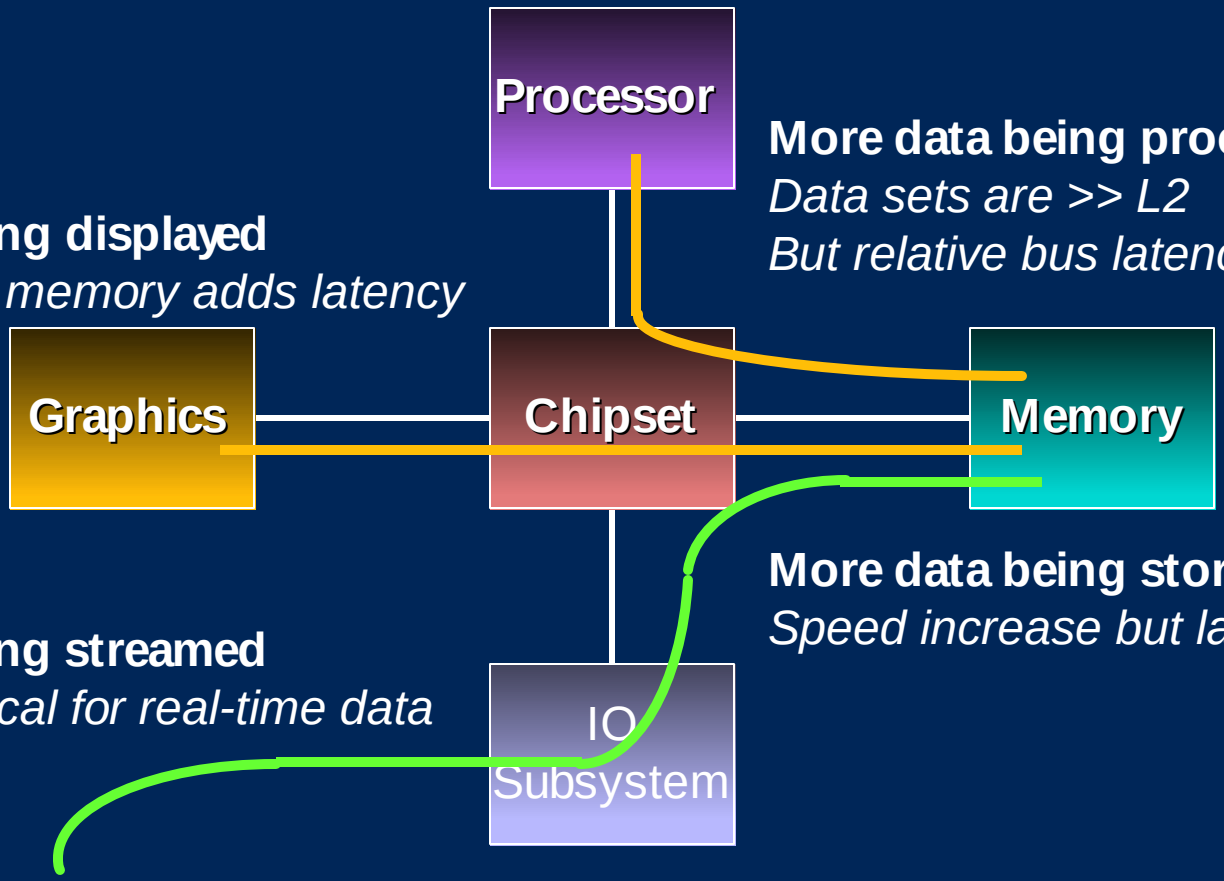
Speed increase but latency constant

More Data Being Streamed



Latency is critical for real-time data

Addressing these Megatrends



More data being displayed
Contention for memory adds latency

More data being processed
Data sets are >> L2
But relative bus latency is increasing

More data being streamed
Latency is critical for real-time data

More data being stored
Speed increase but latency constant

ALL affect the CPU bus architecture!

CPU bus needs to be:

- **Scaleable and latencytolerant**

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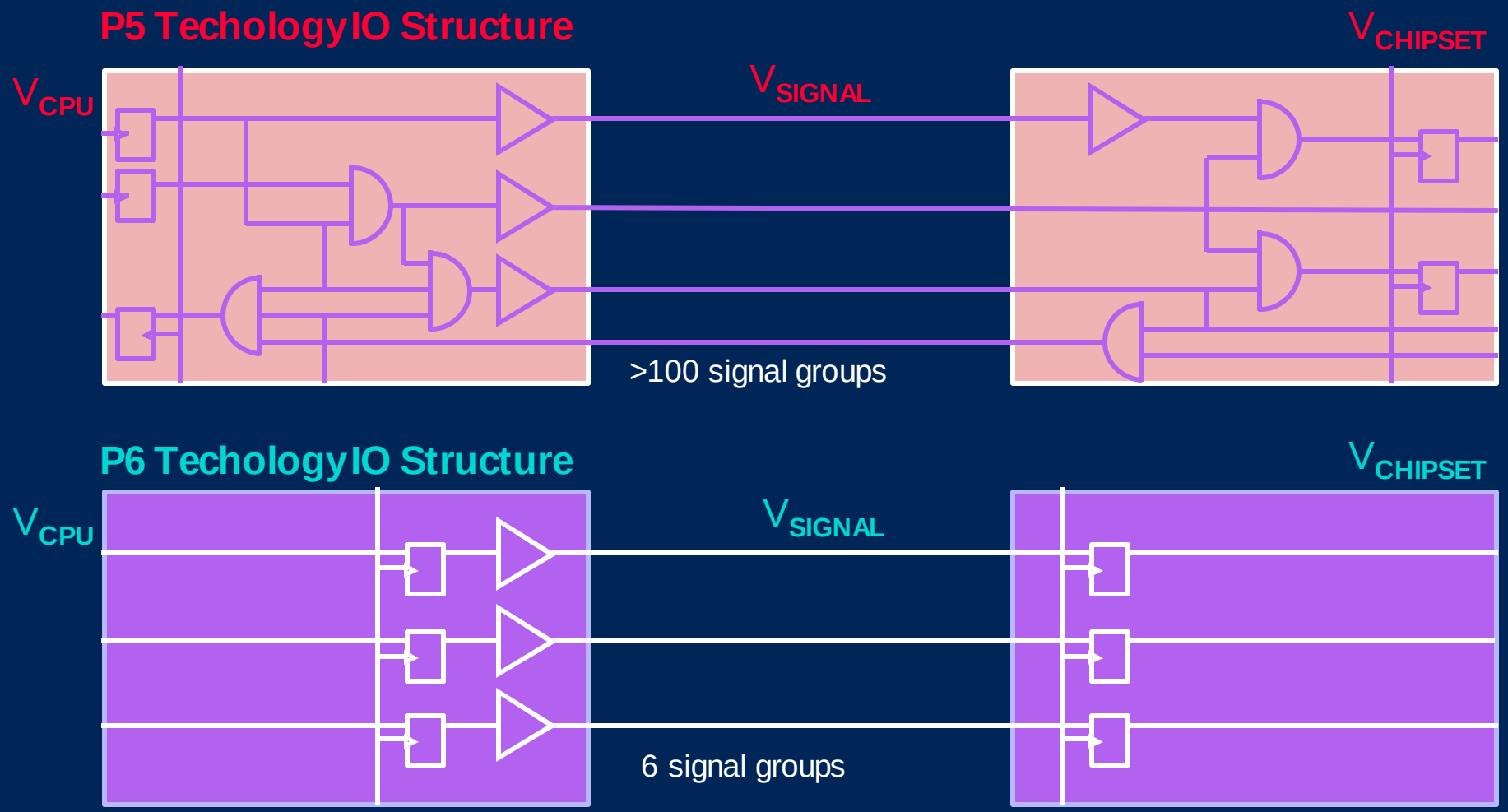
A Scaleable Bus



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Simple, Max. Flight Time, Own Voltage

A latencytolerant bus

Deep pipelining = high throughput + scaleable

66MHz P5 bus

- 325MB/s
  (Maximum sustained read xfer is 4 cachelines/26 clks)

66MHz P6 bus

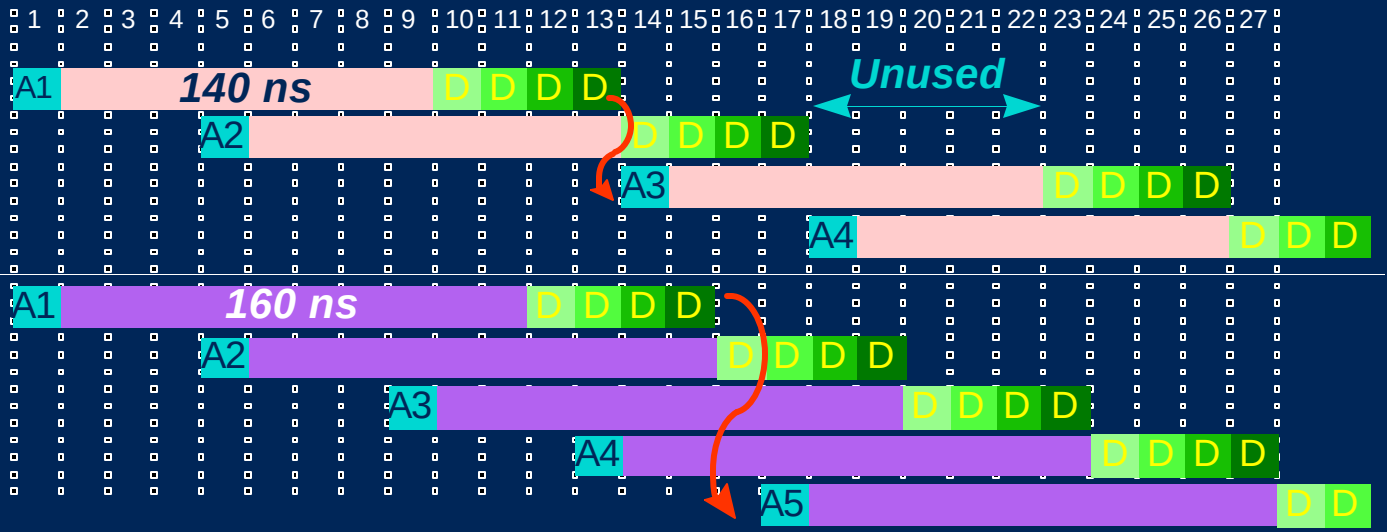
- 533MB/s
  (4 lines/16 clks)

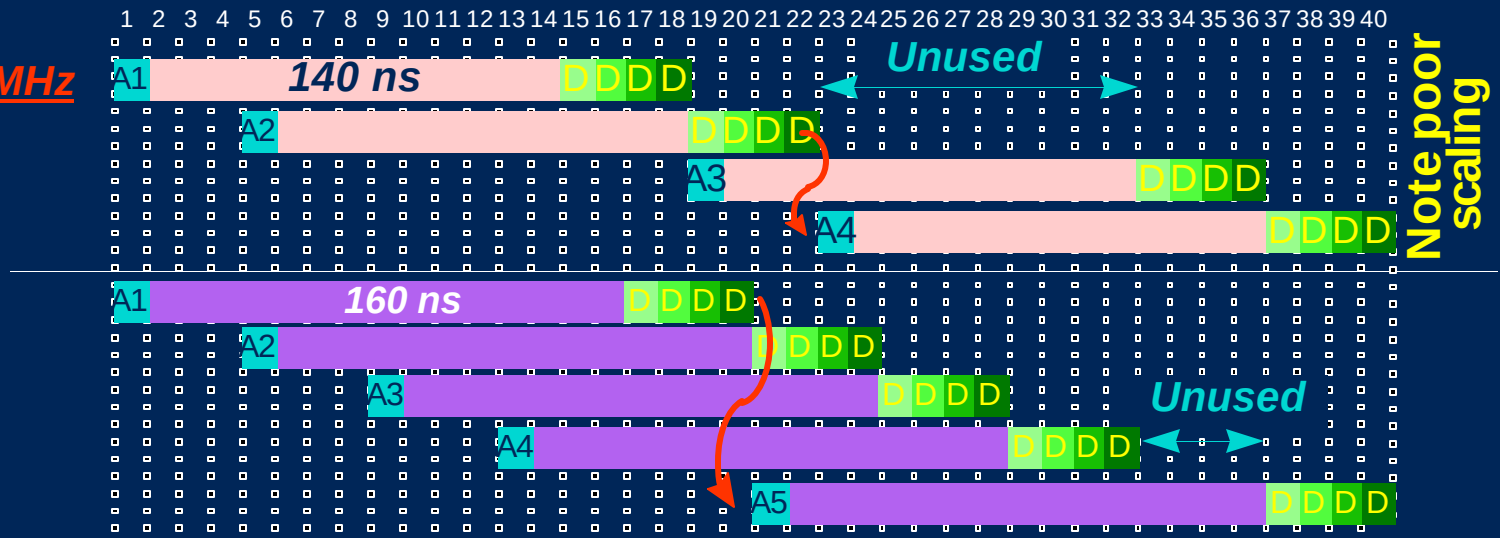
Hypothetical 100MHz P5 bus

- 356MB/s
  (4 lines/36 clks)

100MHz P6 bus

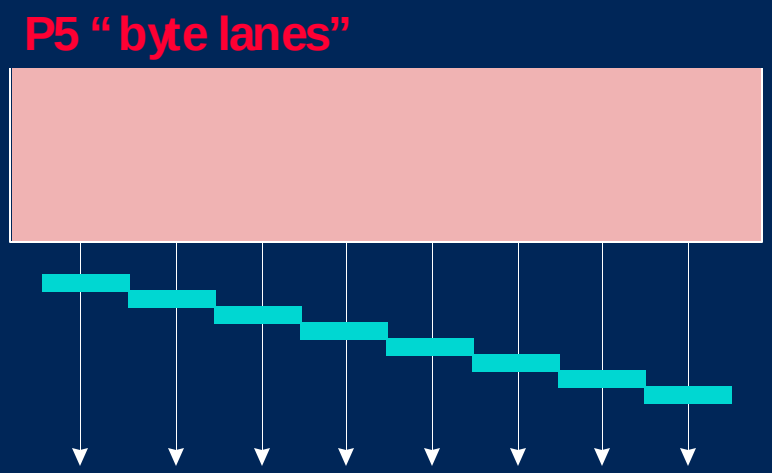
- 640MB/s
  (4 lines/20 clks)

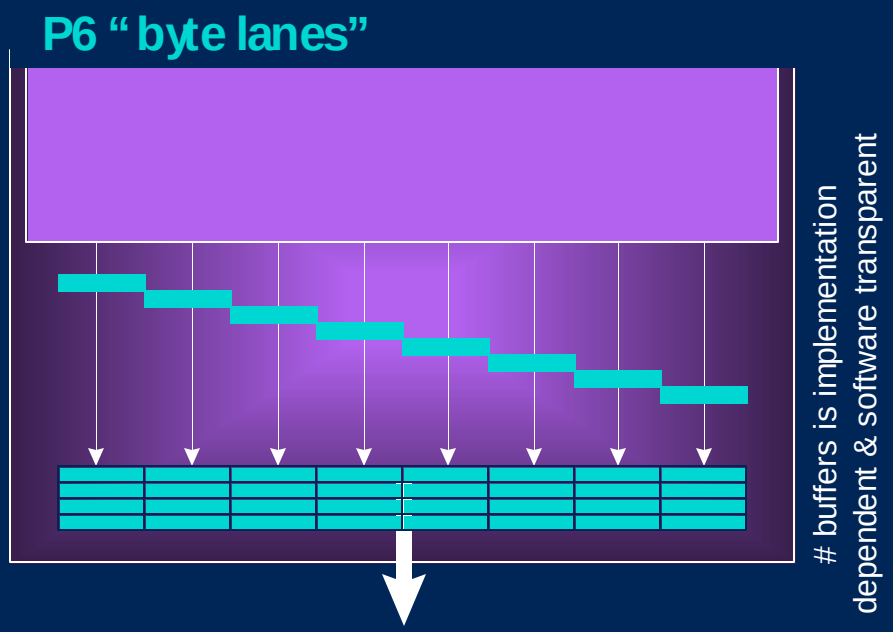




A latencytolerant bus

USWC Memory (Write Combining)





Individual byte/word/dword writes

8 transfers in 44 clks

Minimum cycles chosen on eviction

1 transfer in 15 clks

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Demonstrable Differences

McCalpin STREAMS benchmark*

4 loops that measure memory-system bandwidth

P5 Technology	P6 Technology	
233MHz Pentium® processor	233MHz Pentium II processor	
66MHz Bus	66MHz Bus	
66MHz SDRAM	66MHz SDRAM	Delta
89	126	+41%

* http://www.cs.virginia.edu/stream/
Numbers shown above are averaged across all 4 tests;
Array size used in benchmark = 4M

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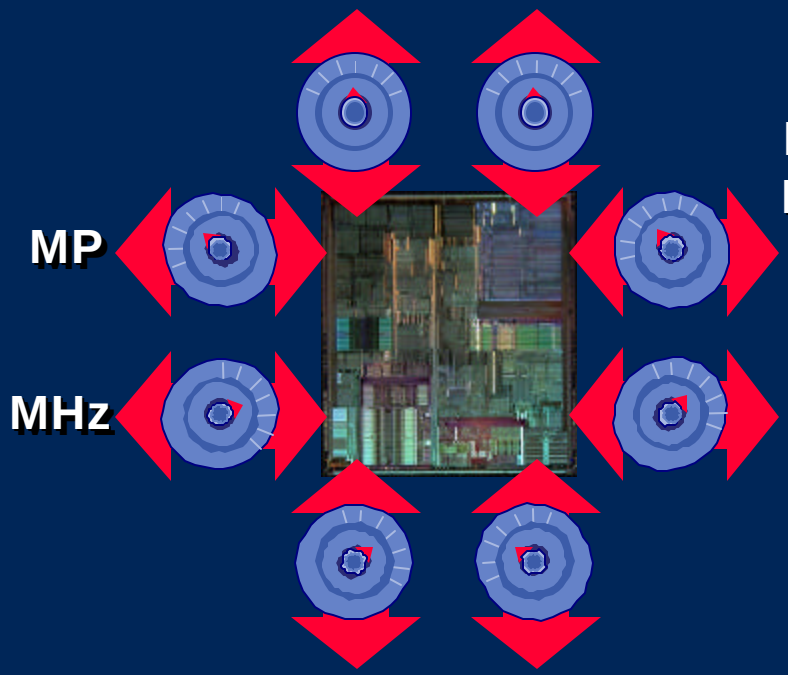
Building on a Solid Foundation



Server and Workstation

Performance PC

Basic PC

Mobile PC

intel® Products for multiple Market Segments

Summary

Future of CPU Bus Architectures

Megatrends demand latencytolerance

- P6 features match design requirements
  - high throughput, scaleable, reliable
- P6 processor core is fast & getting faster
- Graphics moving from 1x AGP to 2x, 4x
- Real time IO traffic will increase
- Memoryspeeds will increase slightly

intel® Intel's future investment is with P6 Bus